

CECS 360 Fall 2016 Project 2

Designing A Testbench

By

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**Lab Description:** This project will require you to characterize and verify the performance of a undefined module. The circuit is a programmable pulse generator with a 16 bit input path. When the load signal is a 1 the data value will be loaded into the circuit. When the load signal is a 0 then the circuit will proceed to generate the desired pulse frequency.

**Verification Report:** The pulse maker is able to create a pulse depended on the data input value ‘din’ and the selected percentage of the duty cycle indicated by the 3-bit selector. The high point of the pulse is when it reaches the data input value and the time when pulse is set to be low is when it has reached the calculated low time, which take into account the select and ‘din’ value.

**Results:** The ‘din’ was altered and based on how long the pulse period. The select altered how long each duty cycle was and the expected low time was equal to din altered by the select value and the case statements. One way to verify the testbench works by taking any of the ‘din’ value within the selector and multiply by the duty cycle.

**(eg.) 000 @ 12.5% duty cycle. din = 4096**

**Expected time = 512**

**4096 \* .125 = *512***

**Problems/Issues:** Test bench isn’t linearly organized compared to other people’s testbenches. The testbench will test all the duty cycles for all ‘din’ cases, and then proceeds to the next duty cycle select. Where as other people test benches are layout as incremental duty cycle selection of one particular ‘din’ and then, reiterates with a new ‘din’ value.

**Sample output:**

ISim P.20131013 (signature 0x7708f090)

WARNING: A WEBPACK license was found.

WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.

WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.

This is a Lite version of ISim.

Time resolution is 1 ps

Simulator is doing circuit initialization process.

0<< Starting the simulation >>

Finished circuit initialization process.

**ISim>**

# run 100us

**ISim>**

# run all

start\_v: 409750

end\_v: 420010

time\_elapsed: 10260

expected\_time: 512\*20 to match our time\_elapsed

din: 4096

start\_v: 2058550

end\_v: 2099530

time\_elapsed: 40980

expected\_time: 2048\*20 to match our time\_elapsed

din: 16384

start\_v: 4966870

end\_v: 5038570

time\_elapsed: 71700

expected\_time: 3584\*20 to match our time\_elapsed

din: 28672

start\_v: 9134710

end\_v: 9237130

time\_elapsed: 102420

expected\_time: 5120\*20 to match our time\_elapsed

din: 40960

start\_v: 14562070

end\_v: 14695210

time\_elapsed: 133140

expected\_time: 6656\*20 to match our time\_elapsed

din: 53248

start\_v: 15104950

end\_v: 15125450

time\_elapsed: 20500

expected\_time: 1024\*20 to match our time\_elapsed

din: 4096

start\_v: 16763990

end\_v: 16845930

time\_elapsed: 81940

expected\_time: 4096\*20 to match our time\_elapsed

din: 16384

start\_v: 19713270

end\_v: 19856650

time\_elapsed: 143380

expected\_time: 7168\*20 to match our time\_elapsed

din: 28672

start\_v: 23952790

end\_v: 24157610

time\_elapsed: 204820

expected\_time: 10240\*20 to match our time\_elapsed

din: 40960

start\_v: 29482550

end\_v: 29748810

time\_elapsed: 266260

expected\_time: 13312\*20 to match our time\_elapsed

din: 53248

start\_v: 30158550

end\_v: 30189290

time\_elapsed: 30740

expected\_time: 1536\*20 to match our time\_elapsed

din: 4096

start\_v: 31827830

end\_v: 31950730

time\_elapsed: 122900

expected\_time: 6144\*20 to match our time\_elapsed

din: 16384

start\_v: 34818070

end\_v: 35033130

time\_elapsed: 215060

expected\_time: 10752\*20 to match our time\_elapsed

din: 28672

start\_v: 39129270

end\_v: 39436490

time\_elapsed: 307220

expected\_time: 15360\*20 to match our time\_elapsed

din: 40960

start\_v: 44761430

end\_v: 45160810

time\_elapsed: 399380

expected\_time: 19968\*20 to match our time\_elapsed

din: 53248

start\_v: 45570550

end\_v: 45611530

time\_elapsed: 40980

expected\_time: 2048\*20 to match our time\_elapsed

din: 4096

start\_v: 47250070

end\_v: 47413930

time\_elapsed: 163860

expected\_time: 8192\*20 to match our time\_elapsed

din: 16384

start\_v: 50281270

end\_v: 50568010

time\_elapsed: 286740

expected\_time: 14336\*20 to match our time\_elapsed

din: 28672

start\_v: 54664150

end\_v: 55073770

time\_elapsed: 409620

expected\_time: 20480\*20 to match our time\_elapsed

din: 40960

start\_v: 60398710

end\_v: 60931210

time\_elapsed: 532500

expected\_time: 26624\*20 to match our time\_elapsed

din: 53248

start\_v: 61340950

end\_v: 61392170

time\_elapsed: 51220

expected\_time: 2560\*20 to match our time\_elapsed

din: 4096

start\_v: 63030710

end\_v: 63235530

time\_elapsed: 204820

expected\_time: 10240\*20 to match our time\_elapsed

din: 16384

start\_v: 66102870

end\_v: 66461290

time\_elapsed: 358420

expected\_time: 17920\*20 to match our time\_elapsed

din: 28672

start\_v: 70557430

end\_v: 71069450

time\_elapsed: 512020

expected\_time: 25600\*20 to match our time\_elapsed

din: 40960

start\_v: 76394390

end\_v: 77060010

time\_elapsed: 665620

expected\_time: 33280\*20 to match our time\_elapsed

din: 53248

start\_v: 77469750

end\_v: 77531210

time\_elapsed: 61460

expected\_time: 3072\*20 to match our time\_elapsed

din: 4096

start\_v: 79169750

end\_v: 79415530

time\_elapsed: 245780

expected\_time: 12288\*20 to match our time\_elapsed

din: 16384

start\_v: 82282870

end\_v: 82712970

time\_elapsed: 430100

expected\_time: 21504\*20 to match our time\_elapsed

din: 28672

start\_v: 86809110

end\_v: 87423530

time\_elapsed: 614420

expected\_time: 30720\*20 to match our time\_elapsed

din: 40960

start\_v: 92748470

end\_v: 93547210

time\_elapsed: 798740

expected\_time: 39936\*20 to match our time\_elapsed

din: 53248

start\_v: 93956950

end\_v: 94028650

time\_elapsed: 71700

expected\_time: 3584\*20 to match our time\_elapsed

din: 4096

start\_v: 95667190

end\_v: 95953930

time\_elapsed: 286740

expected\_time: 14336\*20 to match our time\_elapsed

din: 16384

start\_v: 98821270

end\_v: 99323050

time\_elapsed: 501780

expected\_time: 25088\*20 to match our time\_elapsed

din: 28672

start\_v: 103419190

end\_v: 104136010

time\_elapsed: 716820

expected\_time: 35840\*20 to match our time\_elapsed

din: 40960

start\_v: 109460950

end\_v: 110392810

time\_elapsed: 931860

expected\_time: 46592\*20 to match our time\_elapsed

din: 53248

start\_v: 110802550

end\_v: 110884470

time\_elapsed: 81920

expected\_time: 4095\*20 to match our time\_elapsed

din: 4096

start\_v: 112523010

end\_v: 112850690

time\_elapsed: 327680

expected\_time: 16383\*20 to match our time\_elapsed

din: 16384

start\_v: 115718030

end\_v: 116291470

time\_elapsed: 573440

expected\_time: 28671\*20 to match our time\_elapsed

din: 28672

start\_v: 120387610

end\_v: 121206810

time\_elapsed: 819200

expected\_time: 40959\*20 to match our time\_elapsed

din: 40960

start\_v: 126531750

end\_v: 127596710

time\_elapsed: 1064960

expected\_time: 53247\*20 to match our time\_elapsed

din: 53248

127596712<< Simulation Complete >>

Stopped at time : 127596712 ns : in [File "C:/Users/Z3/Documents/Xilinx Projects - 360/360 - Project 2/CECS360p2/cecs360project2/ProgPulse\_TB.v" Line 105](|C:/Users/Z3/Documents/Xilinx%20Projects%20-%20360/360%20-%20Project%202/CECS360p2/cecs360project2/ProgPulse_TB.v|%20Line%20105%20)